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DESCRIPTION

MEMORY CIRCUIT AND COHERENT DETECTION CIRCUIT

5 Technical Field

The present invention relates to a memory circuit and coherent detection circuit.

Background Art

10 In a CDMA (Code Division Multiple Access)-based mobile communication, the amplitude and phase of an information symbol fluctuate under the influence of Raleigh fading.

15 A "coherent detection system using a pilot symbol" is proposed as a method for carrying out coherent detection by compensating the phase of information symbols on the receiving side.

20 The coherent detection system using a pilot symbol is a method for carrying out coherent detection by estimating fluctuations in the phase of information symbols using pilot symbols (pilot bits) whose phase is known periodically (for example, every 1.25 ms) inserted in an information signal and compensating the phase of the information symbols through interpolation.

25 More specifically, the coherent detection system using a pilot symbol repeats an operation consisting of comparing the phase of a demodulated pilot symbol with an ideal phase (original phase) of the pilot symbol and

calculating the phase error over a plurality of slots, and determines the phase of the information symbol between neighboring pilot symbols from the phase error calculation result through interpolation and thereby 5 carries out coherent detection.

The coherent detection system using a pilot symbol is described, for example, in "Wideband CDMA Open-Air Transmission Result (RCS97-3)".

FIG. 6 shows a configuration example of a reception 10 signal.

A plurality of pilot symbols (pilot bits) 140, 150, 160 and 170 in FIG. 6 are known symbols inserted for every slot.

Detection target slot 2001 is a 1-slot information 15 symbol to be detected. To compensate the phase of this 1-slot information symbol, the amount of phase fluctuation is estimated using pilot symbols over a few slots before and after the detection target slot.

For example, suppose a signal in the configuration 20 shown in FIG. 6 is being received continuously. Suppose a case where coherent detection is performed using a plurality of pilot symbols 140 to 170. In this case, the information symbol which is the target of coherent detection is information symbol 2001 (that is, the 25 detection target slot), two slots ahead of slot 2003 currently being received.

Thus, it is necessary to temporarily store the previously received information symbols (information

symbols up to the one two slots ahead) until the estimation of phase fluctuation using pilot signals (pilot symbols) over a plurality of slots is completed.

That is, a coherent detection circuit requires a
5 memory capable of storing symbols corresponding to at least 3 slots.

On the other hand, a CDMA communication system allows multi-code transmission to speed up communications of large volume image data, etc.

10 Multi-code transmission is a data transmission system intended to effectively use code resources by changing the number of codes to be multiplexed according to the amount of data.

For example, when sound data or a small-volume packet
15 is transmitted, data is transmitted with one spreading code assigned to one physical channel.

On the other hand, when large-volume data such as a motion picture is sent, the motion picture data is divided into a plurality of physical channels, each physical
20 channel is assigned one spreading code and those divided physical channels are multiplexed to carry out data transmission.

Multi-code transmission does not always use all codes, but dynamically determines codes to be used
25 according to the situation. However, it is necessary to secure the memory area necessary to carry out the above-described coherent detection using a pilot symbol assuming the case where all channels are used.

There are various ways of memory configurations and it goes without saying that it is advantageous in every aspect of the area occupied, power consumption and ease of control, etc. to provide a common memory and control 5 the memory in a concentrated manner rather than providing a plurality of memories and controlling them individually.

However, the following problem may arise in the case where electrically continuous memory areas large enough 10 to store all reception data are provided for when the number of multiplexed channels reaches a maximum in order to be able to respond to dynamic changes in the number of multi-codes.

That is, since the same memory area is accessed 15 regardless of the number of multiplexed codes, the entire memory area becomes the access target even in the case where data is transmitted with one code or where a plurality of codes is multiplexed. As a result, power consumption of the memory circuit always remains unchanged.

20 Further, in coherent detection using a plurality of pilot symbols over a plurality of slots, memory accesses occur when the information symbol of a slot currently being received is written and the information symbol of a detection target slot is read. That is, it is not 25 necessary to generate memory accesses for other slots.

However, in the symbol storage memory configuration of a conventional coherent detection circuit, memory areas are electrically continuous, and therefore even

the memory area which need not be accessed may also be accessed and power is wasted accordingly.

The present invention is implemented based on such consideration and it is an object of the present invention
5 to attain low power consumption in a memory circuit and coherent detection circuit.

Disclosure of Invention

The memory circuit of the present invention divides
10 a memory area for strong information symbols into a plurality of electrically separated memory blocks based on at least one of information on the number of multi-codes and slot information.

Then, the memory circuit of the present invention
15 carries out a data write or data read on each of the plurality of memory blocks periodically.

Blocks not subject to any data write or data read are set to a low power consumption mode.

With such a configuration, only necessary memory
20 blocks become access targets first, which reduces the load on the driver and reduces power consumption. Furthermore, forcibly setting memory blocks which need not be accessed to a low power consumption mode (for example, stopping the supply of an operating clock and setting
25 a non-operating state) further enhances the effect of reducing power consumption.

A mode of the memory circuit of the present invention delimits the memory area of the information symbol storage

memory for every code number of multi-code communication and divides it into a plurality of memory blocks. Then, by taking measures such as stopping a clock supply to memory blocks storing information symbols that need not 5 be written or read, the memory circuit of the present invention reduces power consumption.

Furthermore, another mode of the memory circuit of the present invention electrically delimits the memory area for every reception slot and divides it into a 10 plurality of memory blocks. Then, the memory circuit individually generates write access or read access to the memory block corresponding to the detection target slot and the memory block corresponding to the slot currently being received.

15 Furthermore, the coherent detection circuit of the present invention includes the memory circuit of the present invention, an interpolation section that corrects the phases of information symbols through interpolation and a coherent detection section. Since memory power 20 consumption is reduced, power consumption of the coherent detection circuit is also reduced.

A mode of the coherent detection circuit of the present invention electrically delimits the memory area of the symbol storage memory incorporated in the coherent 25 detection section for every multiplexed code and divides it into a plurality of memory blocks. The coherent detection circuit then operates only memory blocks in response to the dynamically variable number of codes.

When the number of codes used is small, the coherent detection circuit forcibly sets memory blocks not in use to a low power consumption mode by stopping the supply of the operating clock, etc. Low power consumption of
5 the circuit is attained in this way.

Brief Description of Drawings

FIG.1 is a block diagram showing an overall configuration of an embodiment of a coherent detection
10 circuit of the present invention;

FIG.2 is a block diagram showing a configuration of a receiver using the coherent detection circuit of the present invention;

FIG.3A illustrates features of a configuration of
15 a memory circuit (symbol storage memory) of the present invention;

FIG.3B illustrates a sequence of write accesses and read accesses of the memory circuit (symbol storage memory) of the present invention;

20 FIG.4A is a block diagram showing a configuration example of the memory circuit (symbol storage memory) of the present invention;

FIG.4B is a circuit diagram showing a configuration example of the memory circuit (symbol storage memory)
25 of the present invention integrated on a single semiconductor chip;

FIG.5 is a flow chart showing a characteristic operation of the memory circuit of the present invention;

and

FIG.6 illustrates a format example of a reception signal used to carry out coherent detection using a pilot symbol.

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Best Mode for Carrying out the Invention

With reference now to the attached drawings, an embodiment of the present invention will be explained
10 in detail below.

(Embodiment 1)

FIG.1 is a block diagram of a coherent detection circuit according to Embodiment 1 of the present invention.

FIG.2 is a block diagram showing a configuration of a
15 CDMA receiver (RAKE combining) using the coherent detection circuit of the present invention.

First, an overall configuration of the CDMA receiver will be explained.

As shown in FIG.2, a CDMA receiver includes reception
20 antenna 7, high frequency signal processing section 8, A/D conversion section 9 that converts an analog signal to digital signal, despreading section 10 that despreads the reception signal at predetermined timing and demodulates data, coherent detection section 11 that
25 carries out coherent detection on the despread data, RAKE combining section 12 that RAKE-combines signals subjected to despreading and coherent detection corresponding to a plurality of paths, channel CODEC section 13 that carries

out channel decoding and multi-code number information extraction section 14 and despreadng code generation section 15.

Despreadng section 10 is provided with a plurality
5 of reception fingers 16a to 16n and searcher 17.

Multi-code number information extraction section 14 extracts information indicating the number of codes inserted in the reception signal and in use and gives this information to coherent detection section 11.

10 Furthermore, despreadng code generation section 15 generates, for example, three despreadng codes C0 to C2 and supplies these codes to despreadng code generation section 15.

A reception signal is demodulated to a baseband
15 signal at high frequency signal processing section 8, A/D-converted to digital data and then input to despreadng section 10.

At despreadng section 10, the reception signal is subjected to despreadng processing by a plurality of
20 despreaders and the data is demodulated. The despreaders are determined taking into account the number of multi-paths and the number of multiplexed codes, etc.

Coherent detection section 11 and RAKE combining section 12 compensate the plurality of data items for
25 the phases of multi-paths for every code and carry out RAKE combining.

Next, a configuration and operation of coherent detection section 11 will be explained with reference

to FIG.1, FIG.3A, FIG.3B, FIG.4A, FIG.4B, FIG.5 and FIG.6.

Coherent detection section 11 shown in FIG.1 temporarily stores the despread data output from reception fingers 16a to 16n in FIG.2, carries out phase
5 compensation and coherent detection.

As shown in FIG.1, coherent detection section 11 includes a plurality of memory blocks 2a to 2i which are physically (electrically) separated from one another, memory interface section 17 (including memory interface
10 circuits 1a to 1c), memory operation control section 3, selector 4, phase estimation section 5, interpolation section 6 and coherent detection circuit 16.

In the figure, BUS 1 to BUS 3 are write buses and BUS 4 to BUS 6 are read buses.

15 Memory blocks 2a to 2i each temporarily store 1-slot information symbol data. Each of memory blocks 2a to 2i corresponds to "one code" and "one slot". That is, the memory area for storing information symbols is divided into a plurality of blocks based on code information and
20 slot information.

In FIG.1, "code unit division" means division of the memory area into three traverse lines. In this way, the memory area is divided into 9 electrically independent memory blocks 2a to 2i.

25 Here, being "electrically independent" specifically means that the word lines are separated from the bit lines.

Dividing the memory area into a plurality of blocks

DRAFT - DRAFT - DRAFT - DRAFT -

allows only necessary blocks to be accessed.

That is, separating the word lines from the bit lines reduces the load on the drivers (word line driver and bit line driver) necessary for memory accesses and reduces 5 the amount of charging/discharging current, making it possible to reduce power consumption.

In addition, forcibly stopping the supply of the operating clock to unused memory blocks makes the main circuit of the relevant block operate in a low power 10 consumption mode. This also reduces the operating current of the circuit, further reducing power consumption.

Memory interface section 17 is a kind of address decoder and determines which address of which memory block 15 should be accessed.

Memory operation control section 3 selects memory blocks to be activated and memory blocks to be set to a low power consumption mode as appropriate, outputs control signals and controls the operating modes of memory 20 blocks.

Memory operation control section 3 is fed with information on the multiplexed code numbers (MCN) output from multi-code number information extraction section 14 in FIG.2.

25 Memory operation control section 3 selects only the memory block line (traverse line) corresponding to the code (multiplexed code) actually being used and deselects other memory block lines.

The selected memory block line is periodically accessed in a predetermined sequence. A specific operating procedure thereof will be described later.

Furthermore, phase estimation section 5 extracts 5 pilot signals inserted at one-slot intervals from each reception signal and estimates the phases of pilot signals on the phase plane (channel estimation).

Interpolation section 6 determines the phase of an information symbol between two neighboring pilot signals 10 through interpolation.

Coherent detection circuit 16 carries out coherent detection on information symbols read from memory blocks at timing corresponding to the phases corrected through interpolation.

15 The signal subjected to coherent detection is given to RAKE combining section 12.

An overall operation of the coherent detection circuit in FIG.1 will be explained more specifically.

Despread information symbols f_0 to f_{n-1} , f_n to f_{2n-1} , 20 f_{2n} to f_{3n-1} are information corresponding to code 1, code 2 and code 3, respectively.

Data corresponding to each code includes n signals from path (0) to path ($n-1$). Signals of different paths have the same information content but have different 25 amounts of delay. Delay differences are on the order of several chips.

Despread information symbols f_0 to f_{n-1} , f_n to f_{2n-1} , f_{2n} to f_{3n-1} are each assigned specific address numbers

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and slot numbers.

The number of addresses of information symbols f_0 to f_{n-1} , f_n to f_{2n-1} , f_{2n} to f_{3n-1} is equal to the number of symbols mapped within one slot of the channel received.

5 Each address of information of f_0 to f_{n-1} , f_n to f_{2n-1} , f_{2n} to f_{3n-1} is given an offset to avoid overlapping. That is, each piece of data is prevented from being written into a same memory space.

Memory interfaces 1a to 1c in FIG.1 are each fed
10 with despread information symbols f_0 to f_{n-1} , f_n to f_{2n-1} ,
 f_{2n} to f_{3n-1} of the same code. That is, despread
information symbols for every path to be subjected to
RAKE combining are input.

Memory interfaces 1a to 1c each serially send
15 information symbols and addresses corresponding to n
paths (n: natural number of 2 or greater) which have been
input in parallel to the write buses (BUS 1 to BUS 3).
As a result, the information symbol data is temporality
stored in corresponding memory blocks 2a to 2i.

20 On the other hand, the information symbol data stored
for a period of time corresponding to 2 slots is selected
by selector 4 and sent to coherent detection circuit 16.

The coherent detection circuit carries out coherent
detection at timing corresponding to the phase
25 compensated by interpolation section 6. The signal
subjected to coherent detection is sent to RAKE combining
section 12 and RAKE-combined there.

Then, with reference to FIG.3A, FIG.3B, FIG.4A and

FIG.4B, the configuration and operation of the symbol storage memories (memory blocks 2a to 2i) shown in FIG.1 will be explained more specifically.

As shown in FIG.3A, the memory area for storing information symbols is divided into three memory block lines (L1 to L3) for the respective codes in order to respond to the case where the code multiplexing number is "3".

Furthermore, the memory area is also divided into three memory block rows R1 to R3 for the respective slots so as to temporarily store information symbols corresponding to three slots while the phase is being estimated from pilot symbols corresponding to two slots before and after the slot to be detected (4 pilot symbols in total). Memory cells are constructed of an SRAM which requires no refreshing.

As a result of such memory area divisions, 9 electrically independent memory blocks 2a to 2i are formed.

That is, the memory area is divided using the number multiplexed codes and slot number as variables. By the way, it is not possible to carry out a read and write on one memory block simultaneously. However, while data is being written to one memory block, data can be read from another memory block at the same time.

Then, the procedure for accessing each memory block will be explained using FIG.3B.

In the following explanations, suppose the number

of multiplexed codes is "1" for convenience of explanations.

When the number of codes is "1", slot number "1" is assigned to a plurality of portions of data (f_0 to 5 f_{n-1}) with different amounts of delay about the information symbol of the first despread slot and the respective portions of data are written to memory block 2a. This state is "state 1".

In FIG.3B, write access is described as "W" and read 10 access is described as "R".

Then, likewise, slot number "2" is assigned to a plurality of portions of data (f_0 to f_{n-1}) with different amounts of delay about the information symbol of the second slot and the data is written to memory block 2b. This 15 state is "state 2".

Furthermore, slot number "3" is assigned about the information symbol of the third slot and the data is written to memory block 2c. At the same time, the data about the information symbol stored two slots ahead is read from 20 memory block 2a. This state is "state 3".

The information symbol data read in state 3 is sent to coherent detection circuit 16 in FIG.1.

Slot number "1" is assigned to the fourth slot data again and the data is overwritten to memory block 2a whose 25 read has been completed. At the same time, the data about the information symbol stored two slots ahead is read from memory block 2b and sent to coherent detection circuit 16 in FIG.1. This state is "state 4".

Likewise, the process moves on to state 5 and then state 6. Since state 6 is the same as state 3, the process moves on to state 4 after state 6, and state 4, state 5 and state 6 appear repeatedly thereafter.

5 Thus, data is written for every slot, in the order of memory block 2a, 2b and 2c. After a write to memory block 2c is completed, the process returns to memory block 2a and a write is performed sequentially again and this procedure is repeated.

10 On the other hand, information symbol data is read starting from the memory block for which a write has completed two slots ahead relative to the memory block currently being written.

15 As is apparent from FIG.3B, not more than two of the three memory blocks operate in the memory block line corresponding to one code in each of states 1 to 6, and therefore there are always memory blocks which need not be operated.

That is, accesses to memory blocks are generated
20 only when information of the "detection target slot" is read and when information of the "slot currently being received" is written.

Therefore, setting memory blocks which need not be operated to a low power consumption mode makes it possible
25 to reduce power consumption. The low power consumption mode of a memory block is implemented by, for example, stopping a clock supply to drive the word lines or bit lines.

The configuration of the present invention can implement operations ① to ④ below.

① It is possible to control so as to prevent write access and read access to a same memory block from occurring simultaneously.

② It is possible to carry out write access and read access to a memory block periodically.

③ It is possible to set a low power consumption mode (non-operating mode) for memory blocks to which no access is generated by stopping the circuit operation or stopping operation of part of the circuit.

That is, it is possible to prevent accesses to memory cells making up the SRAM from being generated. This reduces power consumption to at least two thirds of conventional power consumption.

④ Furthermore, in the example above, only the memory block line corresponding to code 1 (L1 in FIG.3A) operates and memory block lines L2 and L3 corresponding to code 2 and code 3 do not operate at all. This can completely stop the operations of memory blocks 2d to 2i that belong to memory block lines L2 and L3.

In this case, as is apparent from FIG.3A, too, it is only two of the 9 physically (electrically) delimited memory blocks that operate and other memory blocks do not operate.

Therefore, when the number of codes is 1, if power consumption is compared simply focused on the operation ratio, the present invention can reduce power consumption

to two-ninths of the conventional configuration.

Thus, the present invention makes it possible to effectively reduce power consumption of the memory circuit for storing information symbols.

5 Then, the case where the number of multiplexed codes is "2" will be explained.

In this case, memory block lines L1 and L2 operate for code 1 and code 2 respectively and memory block line L3 does not operate. Thus, it is possible to stop the
10 operation of memory block line L3.

Thus, it is 4 of the 9 physically (electrically) delimited memory blocks that operate simultaneously and if power consumption is compared simply focused on the operating ratio, the present invention can reduce power
15 consumption to four-ninths of the conventional configuration.

Likewise, when the number of multiplexed codes is "3", write or read operations occur in all memory block lines L1 to L3. Thus, it is 6 of the 9 physically
20 (electrically) delimited memory blocks that operate simultaneously and if power consumption is compared simply focused on the operating ratio, the present invention can reduce power consumption to six-ninths of the conventional configuration.

25 FIG.4A and FIG.4B show specific configuration examples of memory blocks (for example, 2a to 2c).

Control of switching between operation/non-operation of a plurality of memory blocks

can be implemented as shown in FIG.4A by stopping a clock supply necessary to drive the bit lines and word lines at address decoders 18a, 18b and 18c of the respective memory blocks using a gate circuit, etc.

5 FIG.4B shows a specific circuit configuration. In FIG.4B, memory blocks 2a to 2c are integrated on a single chip. The word lines (w₁ to w_n, w'₁ to w'_{n'}, w''₁ to w''_{n''}) of the respective memory blocks are electrically separated. Likewise, the bit lines are also driven
10 independently.

Driving the word lines and bit lines at the respective memory blocks is controlled by drive circuits 30a, 30b and 30c.

The configuration and operation of memory block 2a
15 will be explained below.

In FIG.4B, a₁ to a_{2n} denote word line (W₁ to W_n) drivers and b₁ to b_m denote bit line (B_{T1} to B_{Tm}) drivers.

Then, drivers (a₁ to a_{2n}, b₁ to b_m) are controlled by drive circuits (30a to 30c) for the respective memories.

20 Therefore, it is possible to individually control active/non-active of each memory by controlling a clock supply at each drive circuit.

As shown above, it is possible to reduce power consumption to two-ninths to six-ninths of that of the
25 memory circuit of the conventional coherent detection circuit by delimiting physically (electrically) the memory area for information symbol storage based on the number of multiplexed codes and slot number.

In the above explanations, the number of multiplexed codes is assumed to be "3", but the present invention is not limited to this. The effect of reducing power consumption of the present invention is enhanced as the 5 number of multiplexed codes increases.

Moreover, in the above explanations, the number of information symbol slots stored is assumed to be 3 slots, but the present invention is not limited to this.

The CDMA receiver shown in FIG.2 has coherent 10 detection section 11 with reduced power consumption, and therefore is suited to LSI implementation. Furthermore, it also allows cellular phone batteries to last longer.

As described above, the characteristic operations of the memory circuit of the present invention can be 15 summarized in FIG.5.

A memory for storage of information symbols is divided into a plurality of electrically separated (electrically independent) blocks based on at least one of the information on the number of multi-codes and slot 20 information beforehand (step 50).

Then, data write and data read are carried out on each of the plurality of blocks periodically while controlling access timing so that write access and read access do not occur simultaneously. Blocks subject to 25 neither data write nor data read are forcibly set to a low power consumption mode (step 51).

Thus, the present invention can minimize power consumption associated with memory accesses by dividing

a memory area into a plurality of blocks and individually controlling operations of the respective blocks. Thus, the present invention allows cellular phone batteries to last longer even if communications of large-volume
5 data such as moving pictures are carried out.

This application is based on the Japanese Patent Application No. 2000-026306 filed on February 3, 2000,
entire content of which is expressly incorporated by
10 reference herein.

Industrial Applicability

The present invention can be applied to a memory circuit or coherent detection circuit mounted on a CDMA
15 receiver.

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